REMARKS

This AMENDMENT UNDER 37 CFR 1.116 is filed with a Request for Continued Examination (RCE) and is further in reply to the outstanding Office Action of January 14, 2004, and is believed to be fully responsive thereto and to place this case in condition for allowance for reasons set forth below in greater detail, and according entry of this AMENDMENT under 37 CFR 1.116 in the RCE is respectfully requested.

Responsive to paragraph 1 of the Office Action, the applicant agrees with the Patent Examiner, and accordingly, each of independent claims 1, 2, 13 and 14 has been amended herein to change "each of the two ends" to – both ends --, as clearly disclosed and taught by the specification.

The explanation in the last two paragraphs of page 10 of the specification is as follows, with underlining added for emphasis.

"The storage capacitors 24 are multi-connected to one Cs line 13 in parallel (similar to Tomita as discussed below), which are illustrated by an equivalent circuit with resistors 42 of the Cs lines 13 as shown in Fig. 4. Therefore, since the rising times of the pulses of the pulse signal Vcs from the Cs line 13 vary depending on the positions of the storage capacitors 24, the above-described Vcs_l varies, thus the quantity of charges stored in each storage capacitor 24 also varies. Fig. 5 shows a relation between the Cs lines 13 and the pulse signals Vcs. In Fig. 5, storage capacitors, TFTs, signal lines, gate lines and the like are omitted. The pulse signals Vcs are applied from the both ends of the Cs line 13. Therefore,

if the Cs line 13 is not disconnected like 'A' line, the rising time of the pulse of the pulse signal Vcs applied to the storage capacitor 24 at the center of the CS line 13 is the longest, and the rising times of the pulses of the pulse signals Vcs applied to the storage capacitors 24 at the both ends of the Cs line 13 are the shortest.

However, in the case where the Cs line 13 is disconnected like 'B' line in Fig. 5, the rising time of the pulses of the pulse signal Vcs 54 applied to the storage capacitor 24 in the vicinity of a disconnected portion 52 becomes long. This is because, even if the pulse signals Vcs are applied from the both ends of the Cs line 13, the pulse signal Vcs stops at the disconnected portion 52 and (only) the pulse signal Vcs from the reverse direction is applied. Accordingly, this causes some storage capacitors 24 to store different quantities of charges from the ones stored in the storage capacitors 24 when the Cs line 13 is not disconnected."

It is this principle of operation that the present invention takes advantage of in detecting the presence of a disconnected storage capacitor line.

Moreover, this principle of operation is now specified in greater detail in each of independent claims 1, 2, 13 and 14 by specifying, after applying pulse signals from both ends of said plurality of capacitor lines to said plurality of storage capacitors such that in a connected storage capacitor line the storage capacitors located near each end of the storage capacitor line have a stored voltage whch rises relatively fast and the storage capacitors located near the center of the storage capacitor line have a stored voltage which rises relatively slowly compared to the storage capacitors located near each end of the storage capacitor line, and in a disconnected storage capacitor line having a disconnection, storage

capacitors located near the disconnection have a stored voltage which rises relatively slowly compared to similarly located storage capacitors in a connected storage capacitor line.

Reconsideration is respectfully requested of the rejection of claims 1-12 and 13-14 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomitan (sic. Tomita) ('061).

The present specification clearly explains "the pulse signal Vcs being applied from both ends of the Cs line 13" through elements 28 as shown in Figure 5 (on page 10, lines 19-21 in specification). Moreover, this application from both ends of the Cs line 13 is such that in a connected storage capacitor line the storage capacitors located near each end of the storage capacitor line have a stored voltage whch rises relatively fast and the storage capacitors located near the center of the storage capacitor line have a stored voltage which rises relatively slowly compared to the storage capacitors located near each end of the storage capacitor line, and in a disconnected storage capacitor line having a disconnection, storage capacitors located near the disconnection have a stored voltage which rises relatively slowly compared to similarly located storage capacitors in a connected storage capacitor line. This configuration of Fig. 5, as specified by each of independent claims 1, 2, 13 and 14, is a major distinguishing feature of the present invention which the combination of prior art does not disclose or teach.

Tomita discloses and teaches a two-capacitor system on each pixel circuit (as shown in Figure 1). However each of the capacitors C1 and Cs is connected to counter-electrode 91 and storage capacitor line 52, respectively, and is driven by counter electrode

driving circuit 20 and storage capacitor line driving circuit 21, respectively. As a result, Tomita does not teach a pulse signal generating device 21 connected to both ends of each of storage capacitor lines, since each storage capacitor line has only one end with a connection with other Cs lines (Figures 1, 5 of Tomita).

Neither Suzuki et al nor Tomita discloses or teaches such a test method wherein a test pulse is applied to both ends of the storage capacity line, with the realization that if the storage capacity line is disconnected, the rising times of the storage waveforms is affected, and times of the storage waveforms of the storage capacitors in the vicinity of the break are the longest compared to similarly located storage capacitors in a connected storage capacitor line, which enables the presence of the break to be detected.

This mode of operation is simply not disclosed or taught by either Suzuki et al or Tomita.

The Final Rejection states that "Tomitam (sic)('061) does teach "applying pulse signals from each of the two ends of said plurality of storage capacitor lines (52) to said plurality of storage capacitors (61) as claimed since Tomitam (sic)('061) teaches his plurality of storage capacitors (61) are multi-connected to one capacitor line (52) in parallel (see Fig. 1) which is similar to applicant's circuitry shown in Fig. 8."

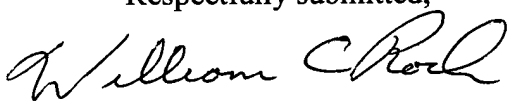
It is true that Tomita has a plurality of storage capacitors connected multi-connected to one capacitor line in parallel. However, the storage capacitance line driving circuit 21 applies a high voltage to only one end of each storage capacitor line 52, which high

voltage and charging current propagates down the storage capacitor line 52 to multi-connected capacitors along the line 52 in a manner as described above with respect to the present invention. It is this finite propagation time down the storage capacitor line 52, which cause storage capacitors closest to the connection end to charge faster and cause storage capacitors furthest from the connection end to charge more slowly, that the present invention takes advantage of.

Accordingly, even though Tomita discloses a plurality of storage capacitors (61) multi-connected to one capacitor line (52) in parallel and a pulse signal generating device (21) connected to one end of each the plurality of storage capacitor lines (52), Tomita does not apply pulse signals from both of the storage capacitor lines.

This application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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